

CIBSOC Program – Spiral Inductor Inductance Calculation and Layout Optimization

Claudia Pacurar¹, Vasile Topa¹, Adina Racasan¹, Calin Munteanu¹

¹Technical University of Cluj-Napoca, 26-28 Baritiu Street, Romania, Claudia.Pacurar@et.utcluj.ro; Vasile.Topa@et.utcluj.ro; Adina.Racasan@et.utcluj.ro; Calin.Munteanu@et.utcluj.ro

Summary Spiral inductors are very often used in integrated circuits for many applications. To design spiral inductors or to improve the spiral inductors performances is absolutely necessary to calculate their inductances and/or to optimize their layouts. In this effect we create a software program, named CIBSOC (Spiral Inductors Inductance Calculation and Layout Optimization). The program is dedicated to calculate dc inductances and to optimize layouts for spiral inductors. We use a wide range of inductors in the applications made with our program. We compare the results of our applications with the measurements results existing in the literature and also with the results that we have obtained using a commercial field solver in order to validate our program. Our program is accurate enough, has a very friendly interface, is very easy to use and it calculates the problems in a very short running time compared with other similar programs. Since spiral inductors tolerance is generally on the order of several percent, a more accurate program is not needed in practice. The program is very useful for the spiral inductors design, because it calculates the inductance of spiral inductors with a very good accuracy. It is also useful for the spiral inductors optimization, because it affords optimal solutions for spiral inductor layouts in terms of the technological limitations and/or of the users' needs.

1. Introduction

The passive components parameters extraction from radio frequency integrated circuits such as inductance, capacitance and resistance extraction are research topics of great interest and also very provocative. This fact is motivated by the continual technological progress thanks to it is now possible to implement integrated circuit at microns dimensions. The minimization of the integrated circuit dimensions at this extreme level lead in an implicit way to the significant rise of parameters extraction importance. These parameters must be calculated with a very good accuracy. We focus on inductance calculation. The inductance value extraction was and is intensely studied in the literature. At this moment exists many expressions and methods used for integrated circuits inductance extraction [1]-[5],

but as is mentioned in the literature, there are limits in their application.

2. CIBSOC Software Program

To design and to optimize the spiral inductors from integrated circuits is first necessary to find the exact parameters values, such as inductance value. So the fast and accurate inductance extractions become more and more important for design, optimization and design verification of the spiral inductors and for their performances improvement. The exact inductance calculation for spiral inductors; the spiral inductors optimization by finding their optimal layout for a given maximal inductance or for any given inductance value keeping a constant area for the inductor implementation in the integrated circuits are still needed to improve the spiral inductors performances. To this aim we implement a software program that allow fast and accurate inductance calculation and spiral inductor layout optimization. The program is composed of four modules. The first and the second one are created to calculate the spiral inductor inductance. The third and the fourth one are created to optimize the spiral inductor layout.

3. Applications in CIBSCO Program

We create a set of spiral inductors and we implement them in our program to find their inductances and to optimize their layouts. We present in this paper only the spiral inductors with square shape, even if the program allows also the calculation for hexagonal, octagonal and circular shapes of spiral inductors. We use CIBSOC program to calculate the total inductance for each of the square spiral inductor that we create and to optimize their layouts. All the dimensions used in the paper are in [μm] and the inductance values in [nH].

4. Comparison with Measurements

We calculate the inductance for some square spiral inductors that exist in the literature with measurements results (Table I) and we compare these results with the results obtained with our program. We demonstrate the accuracy of our CIBSOC program results.

Table I
Comparison of our results with measurements results

N (turn)	Ref.	d_c (μm)	w (μm)	s (μm)	t (μm)	L_m (nH)	L_{CIBSOC} (nH)	ϵ_r (%)
2.75	[6]	279	18,3	1,9	0,9	3,1	3,009	2,93
7.50	[6]	166	3,2	1,9	0,9	12,4	11,987	3,33
9.50	[6]	153	1,8	1,9	0,9	18,2	17,842	1,96
2.75	[6]	277	18,3	0,8	0,9	3,1	3,055	1,45
5.00	[6]	171	5,4	1,9	0,9	6,10	5,859	3,95
3.75	[6]	321	16,5	1,9	0,9	6,1	6,026	1,21
3.00	[7]	300	19	4	0,9	3,3	3,4977	5,99
5.00	[7]	300	24	4	0,9	3,5	3,7736	7,81
9.00	[7]	230	6,5	5,5	0,9	9,7	9,6791	0,21
8.00	[8]	226	6	6	0,9	9,00	9,143	1,58
16.00	[8]	300	5	4	0,9	34	36,544	7,48
6.00	[7]	300	9	4	0,9	11,7	12,444	6,36

5. Comparison with Commercial Field Solver

To validate our CIBSOC program we consider a very good opportunity to use a demo version of a commercial field solver dedicate to the parameters extraction from different types of complex integrated circuits. We implement in this program a wide range of square spiral inductors starting with the one that we create. The results of inductance variation in terms of the number of turns are presented in Table II.

Table II
Comparison of Results. Inductance vs. number of turns.

Number of turns	L_{CIBSOC} (nH)	$L_{\text{commercial program}}$ (nH)
1	1,808	1,7309
2	5,582	5,4228
3	10,527	10,285
4	16,15	15,833
6	28,081	27,637
8	39,347	38,794
12	55,315	54,704
16	60,064	59,646

The inductance variation in terms of the number of turns is plotted in Fig. 1. We observe close agreement between the results. With dotted line

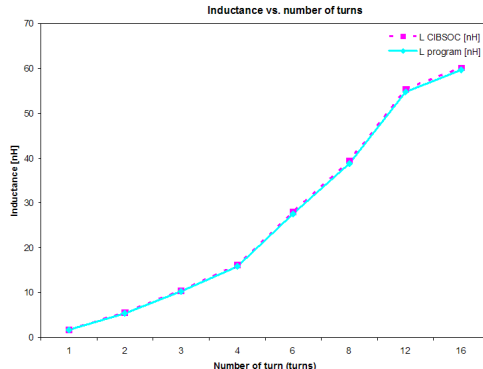


Fig. 1. The comparison of the results obtained with CIBSOC program, and respectively with the parameters extraction program.

are plot the results obtained with our CIBSOC program, and with continuous line the results obtained with the commercial program.

6. Conclusions

The main aim of this paper was to present the inductance calculation and layout optimization for spiral inductors CIBSOC software program implemented by the authors. The program validation was done by comparison of the results obtained with our CIBSOC program, with the measurements results taken form literature and respectively with the results obtained by modeling the square spiral inductors also with a commercial field solver create especially for parameters extraction. Analyzing the results obtain on these three different ways we ascertain the results similitude, the small errors that prove the accuracy of our program. We consider our program very useful for design and for optimization of spiral inductors. It is easy to use and the running times are small compared with other similar programs. We want to extent our program also for ac parameters calculation, at high frequency.

References

1. C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, *A physical model for planar spiral inductors on silicon*, in Proceedings IEEE IEDM'96, 1996.
2. J. Crols, P. Kinget, J. Craninckx, and M. Steyeart, *An analytical model of planar inductors on lowly doped silicon substrates for analog design up to 3GHz*, in Symposium on VLSI Circuits, Digest of Technical Papers, 1996, pp. 28-29.
3. H. M. Greenhouse, *Design of planar rectangular microelectronic inductors*, IEEE Transactions on parts, hybrids, and packaging, vol. PHP-10, no. 2, pp. 101-109, 1974.
4. H. A. Wheeler, *Simple inductance formulas for radio coils*, Proceedings of the IRE, vol. 16, no. 10, pp. 1398-1400, October 1928.
5. H. E. Bryan, *Printed inductors and capacitors*, Teletech and electronic industries, 1955.
6. J. J. Zhou and D. J. Allstot, *Monolithic transformers and their application in a differential CMOS RF low-noise amplifier*, IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 2020-2027, 1998.
7. K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moianian, *High Q inductors for wireless applications in a complementary silicon bipolar process*, IEEE Journal of Solid-State Circuits, vol. 31, no. 1, pp. 4-9, 1996.
8. J. N. Burghartz, K. A. Jenkins, and M. Soyuer, *Multilevel-spiral inductors using VLSI interconnect technology*, IEEE Electron device letters, vol. 17, no. 9, pp. 428-430, 1996.